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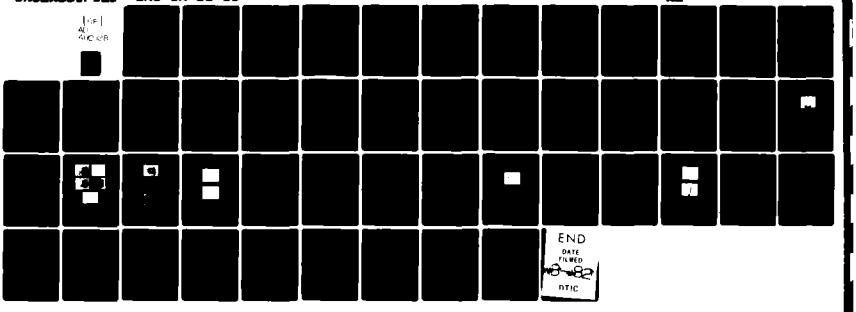

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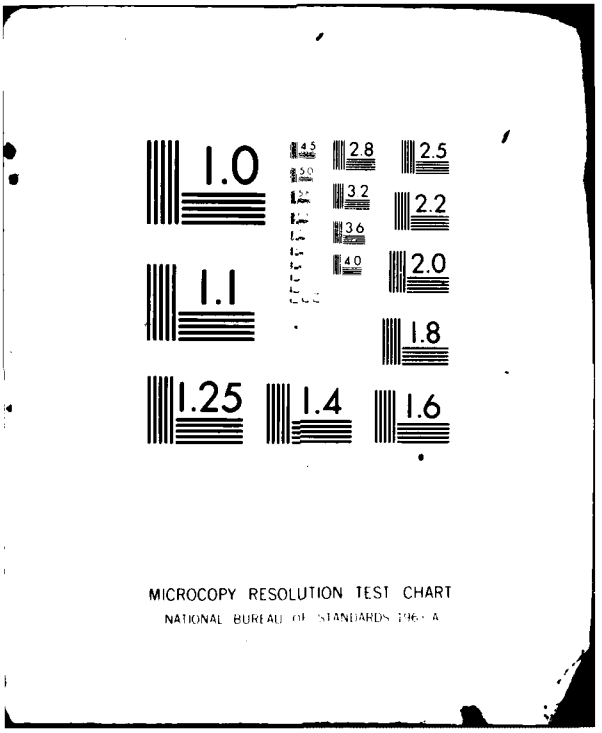
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NIOBIUM NITRIDE JOSEPHSON DEVICES WITH SEMICONDUCTOR BARRIERS

H. Kroger, D. W. Jillie and L. N. Smith
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Semiconductor barriers are investigated as a means of producing NbN-barrier-NbN and NbN-barrier-Nb Josephson devices. Chemical vapor deposition of silicon and germanium polycrystalline barriers onto NbN substrates and sputter deposition of amorphous silicon onto NbN substrates were used to produce the barrier layers. NbN-aSi-Nb tunnel junctions which had a V_m (product of critical current and subgap resistance) as high as 15 mV were fabricated. Phosphorus doped Ge barriers about 60 Å thick produced tunnel junctions with V_m = 2-3 mV. Super Schottky diodes were produced with boron doped germanium barriers about 130 Å —

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thick. Boron doped germanium barriers about 60-70 Å thick were observed to have Josephson coupling with good uniformity as judged by ideal threshold curves, but had non-ideal tunneling characteristics. NbN-Ge-NbN devices were produced by first depositing the trilayer layer structure over the entire wafer and then isolating the desired junctions by thermally oxidizing the upper NbN layer between devices, with the device area being protected from oxidization by a patterned SiO_2 layer. Some correlation between good tunneling characteristics and the crystal structure and high optical reflectivity of the lower NbN electrode was observed.

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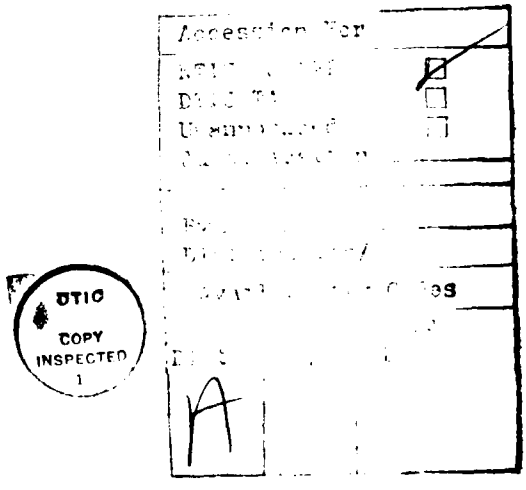

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SECTION I

INTRODUCTION

The general purpose of this program is to develop a Josephson device technology which will permit the operation of Josephson devices at 8-10^{o}K or higher. Operation of Josephson devices at such high temperatures would permit cooling by presently available closed cycle refrigerators with no liquid helium required. This could eventually be important to the Navy in insuring reliability and the maintainability in future applciations of Josephson devices in military systems.

The specific approach of this program was to concentrate on the study of deposited polycrystalline semiconductor barriers with niobium nitride (NbN) electrodes which have a superconducting transition temperature of 15-16^{o}K. There are several potential advantages of NbN-c semiconductor-NbN sandwich devices. These include:

(1) The opportunity to use a possibly low capacitance barrier.

(2) The specific use of crystalline rather than amorphous semiconductors might enable a more complete understanding of the electronic properties of the barrier. Crystalline semiconductors are far better understood than are amorphous semiductors.

(3) The methods of depositing c-Ge and especially c-Si are part of a highly developed technology in the semiconductor industry.

(4) The superconducting quality of NbN films (and many other "exotic" compound high-T_c materials) is partially controlled by a requirement to heat the substrate during deposition. Deposition of a barrier at a relatively high temperature by chemical vapor deposition (CVD), for example, ensures that the barrier material will not change during the subsequent deposition of the NbN counterelectrode. Such a change might occur if an amorphous semiconductor layer were deposited

(a-Si may crystallize at 600-700°C, for example). Of course, there are other means of ensuring that disruption of a barrier will not take place during the deposition of the counterelectrode. A partial oxidation of an amorphous Si barrier might have helped prevent the destruction of the barrier in the NbN-SiO_x-NbN devices described by Shinooki et al.[1]

(5) The classic crystalline semiconductor barrier devices are thin single-crystal silicon membranes as fabricated by the Berkeley Group.[2,3] Undoubtedly, these single-crystal barriers are inherently somewhat better understood than the polycrystalline barriers described in this report, but they are both more fragile and more difficult to fabricate than deposited barriers.

The methods of fabrication of devices investigated during the course of this program are described in detail in Sec. II. The interpretation of the characteristics of these devices is presented in Sec. III. The relationship between device properties and the various methods of fabrication is also discussed in Sec. III. A summary of the work is presented in Sec. IV. This summary includes a discussion of potentially valuable future investigations.

II. DEVICE FABRICATION

A. Device Structures

(1) "First Stage" Devices. It may be useful to point out that chronologically this work can be divided into three stages. The first stage began with the observation that Si and Nb undergo a surface reaction at about $300^{\circ}C$ causing a disruption of a Si barrier, whereas most Si barriers deposited on NbN do not react till temperatures of $\approx 800^{\circ}C$ are attained. This observation permitted the deposition of c-Si by conventional CVD techniques at $\approx 725\text{-}760^{\circ}C$. Devices studied in this first stage were made by depositing Si onto SiO_2 windows previously deposited and patterned on a NbN film, as shown in cross section in Fig. 1. We shall refer to this fabrication scheme as the "conventional" process.

The SiO_2 was deposited by sputtering and the patterning of the windows in the SiO_2 was accomplished by etching in buffered HF. Wet etching (rather than, say, reactive sputter etching) was purposefully used in order to introduce an extended taper to the edges of the window. This taper was desired in order permit as uniform coverage of the open NbN area as possible. Previous experience in depositing thin Si tunneling barriers (on semiconducting, not superconducting devices) indicated that nonuniform coverage was a potential problem. Examination with an optical microscope revealed no nonuniformity, but this is not a sensitive test. In this first stage of the investigation the device dimensions were relatively large, from 12 X 25 μm to 25 X 50 μm.

(2) "Second Stage" Devices. Three changes occurred in the "second-stage" device fabrications. The CVD barrier layers were deposited onto an uncovered, unpatterned NbN layer; lower temperatures were used to deposit Si layers and Ge layers were also deposited onto NbN at even lower temperatures; much smaller area devices were used (as small as 4 μm X 4 μm).

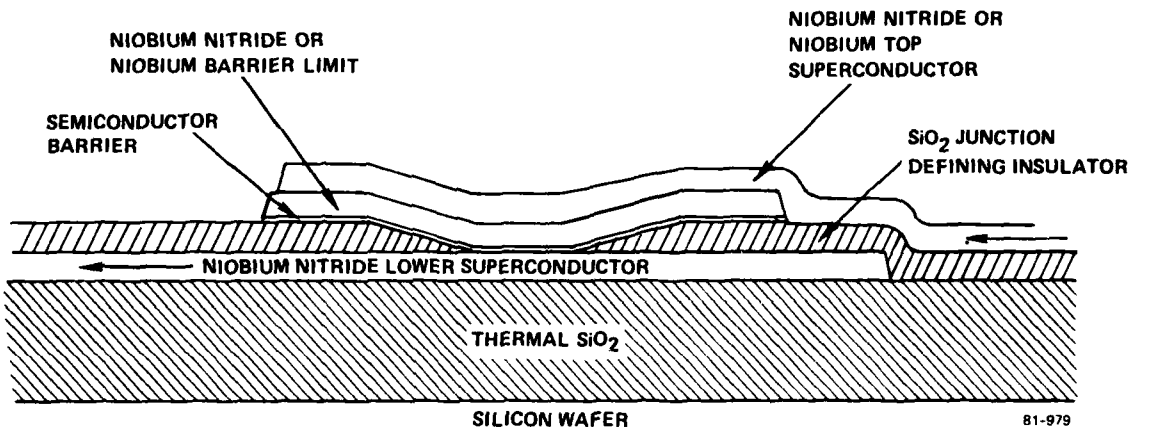

FIG. 1 Cross-sectional diagram of "first-stage" conventional device structure. Note that SiO_2 layer is deposited and patterned before barrier.

The desired method of fabricating NbN-c-semiconductor-NbN devices is illustrated in Fig. 2, which shows device cross sections at various stages in the fabrication process. This fabrication method is an obvious adaptation of our SNAP (selective niobium anodization process) procedure[4] which has been used for Nb-Si-Nb and Nb-Nb_2O_5-Nb devices. The distinctive feature of this fabrication procedure is that an entire trilayer sandwich of NbN, semiconductor and NbN is produced, as shown in Fig. 2, before any photoresist steps are performed. The active device areas are then selected by patterning of $\lesssim$1000 Å SiO_2 layer which prevents the oxidization of NbN counterelectrodes where we choose to form devices. Isolation of individual devices is obtained by the complete consumption by oxidation of the upper (counterelectrode) NbN layer in the region between devices.

The use of anodization, rather than oxidization, to isolate individual devices, is not desirable for a NbN counterelectrode because of the difficulty in forming a continuous, uniform anodized NbN layer.[5] This will be described below in Sec. II D in more detail. Anodization, however, provides for an in-process determination of when the complete consumption of the upper electrode is accomplished.[4] However, the procedure for isolation by anodization was useful for the majority of devices fabricated on this project. This is because of the desirability of often fabricating NbN-semiconductor-Nb devices. Such devices permit a partial concentration on the properties of the NbN-semiconductor interface since the properties of the semiconductor-Nb interface can often be inferred from auxiliary experiments which involve Nb electrodes exclusively. The processing of a NbN-semiconductor-Nb device is essentially identical to the SNAP procedure. Minor modifications in interpretation of the end-point due to the presence of, perhaps, a degenerately doped Ge barrier are discussed below in Sec. II D. The process sequence for fabrication of a NbN-semiconductor barrier-Nb device is shown in Fig. 3, which is essentially identical to the SNAP.

There are several advantages to this general method of fabrication:

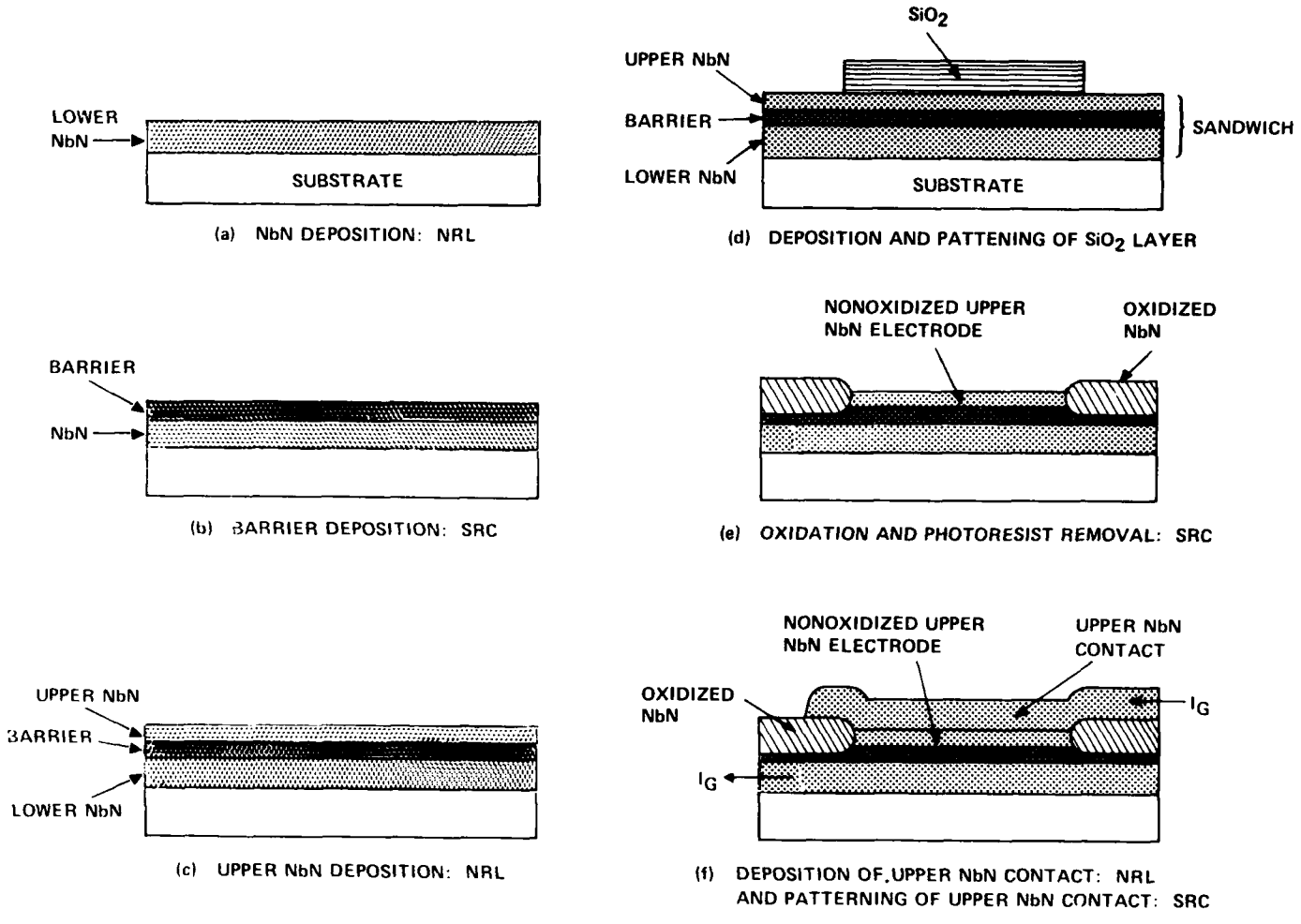

FIG. 2 Device processing sequence for NbN devices developed on this program. Note that superconductor-barrier-superconductor trilayer is formed before patterning of any layer.

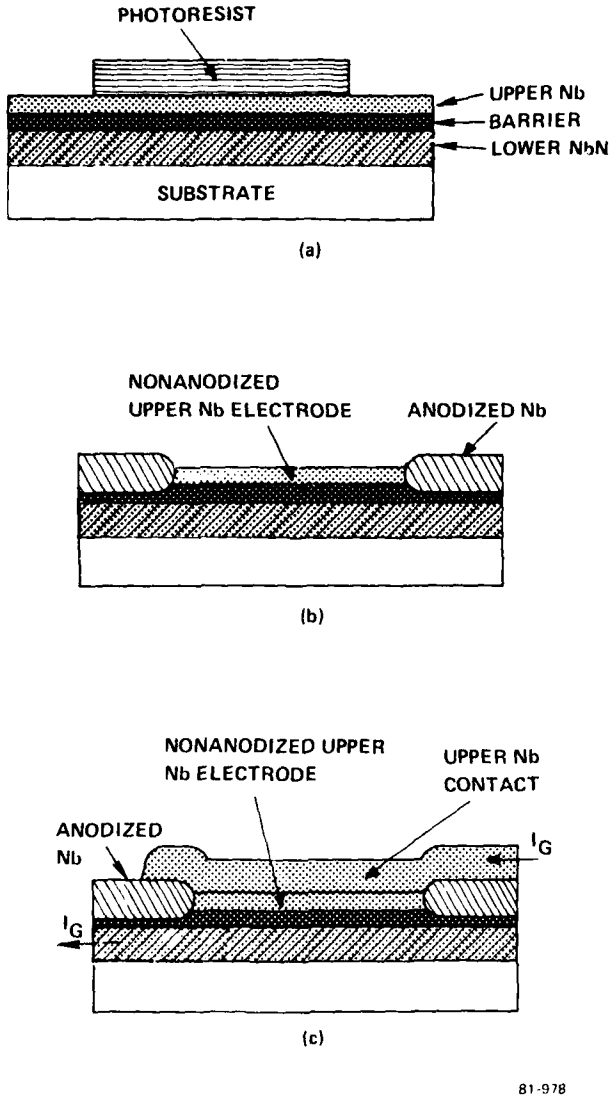

FIG. 3 SNAP device fabrication sequence for NbN-S-Nb devices.

(1) Since there are no intervening photoresist or electron resist steps, the method is capable of extraordinary cleanliness.

(2) Since the deposition of the barrier layer is on a truly plane (nonpatterned) surface, greater uniformity can be expected. This expectation is especially valid for CVD barriers where the natural flow of the reactant gases could cause an assymetry between the upstream and downstream sides of previously patterned windows.

(3) This procedure permits a rapid turn-around of devices because only two photoresist steps are required.

(4) This method of fabricating NbN-semiconductor-NbN or NbN-semiconductor-Nb devices permits a convenient, useful and meaningful comparison with Nb-Si-Nb devices which are being developed independently of this program.

The use of lower temperatures for CVD of Si was instituted during the "second stage" in order to emulate the work of Taniguchi et al.[6] This will be discussed below in Sec. II B. Smaller area active devices were used in order to not have such large supercurrents that switching of electrodes to the normal state could occur.

(3) "Third Stage" Devices. The "third stage" of this work used sputter-deposited amorphous Si layers and Nb counterelectrodes. The use of such structures served to make contact with other work at SRC on Nb-Si-Nb SNAP devices which by this time had attained a high level of reproducibility. This structure permitted not only an Ar sputter clean of the barrier before the Nb counterelectrode was deposited, but deposition of the silicon barrier in almost the identical manner of high quality Nb-Si-Nb devices. We felt that a comparison with this work was valuable because we observed correlations between the quality of the junctions and the T_c of the NbN layers on which the semiconductor barriers were deposited. Falling back on our most tested barrier material might more firmly establish this correlation. The structure of these devices has already been shown in Fig. 3.

B. Barrier Depositions

(1) Chemical Vapor Depositions: Apparatus and General Procedure. The silicon and germanium chemically vapor-deposited layers were produced by the pyrolysis of silane or germane in a room pressure cold wall reactor which is diagrammed in Fig. 4. The temperature of the graphite susceptor can be monitored and controlled by an infrared pyrometer which is not shown in the diagram. The operation of the reactor, including the timed sequences of both gas flow and temprature, can be preprogrammed to ensure reproducibility.

For many of the silicon and germanium depositions, a relatively small graphite susceptor was used. A small susceptor was found useful to more accurately control the temperature of deposition in this reactor, especially at lower temperatures, as schematically indicated in Fig. 4. The NbN wafer is surrounded by closely spaced silicon wafers which had previously been coated by CVD Si_3N_4 layers.

Several polysilicon etches, including HF + CrO_3 + H_2O mixtures, can serve as rapid etches of polysilicon or polygermanium without significantly attacking the Si_3N_4. This permits the relatively accurate measurement of the thickness of deposited semiconductor layers. The thickness of the deposited layers can be determined, if a steep step is etched, by multiple beam interferometry, or, if thicker layers are used by a Dec-Tac mechanical measurement.

Almost all of the NbN layers used in this study were deposited by reative sputtering at the Naval Research Laboratory by E. Cukauskas. (A few NbN layers were deposited at Sperry Research Center, but since these had a transition temperature $T_c \leq 9^oK$, and we learned that a high T_c was important for obtaining good quality junctions, the SRC layers were not used except occasionally for process development.) In order to attempt to ensure the highest quality NbN-semiconductor interface and reproducibility, almost all NRL layers were subjected to the following treatment before a semiconductor barrier was deposited:

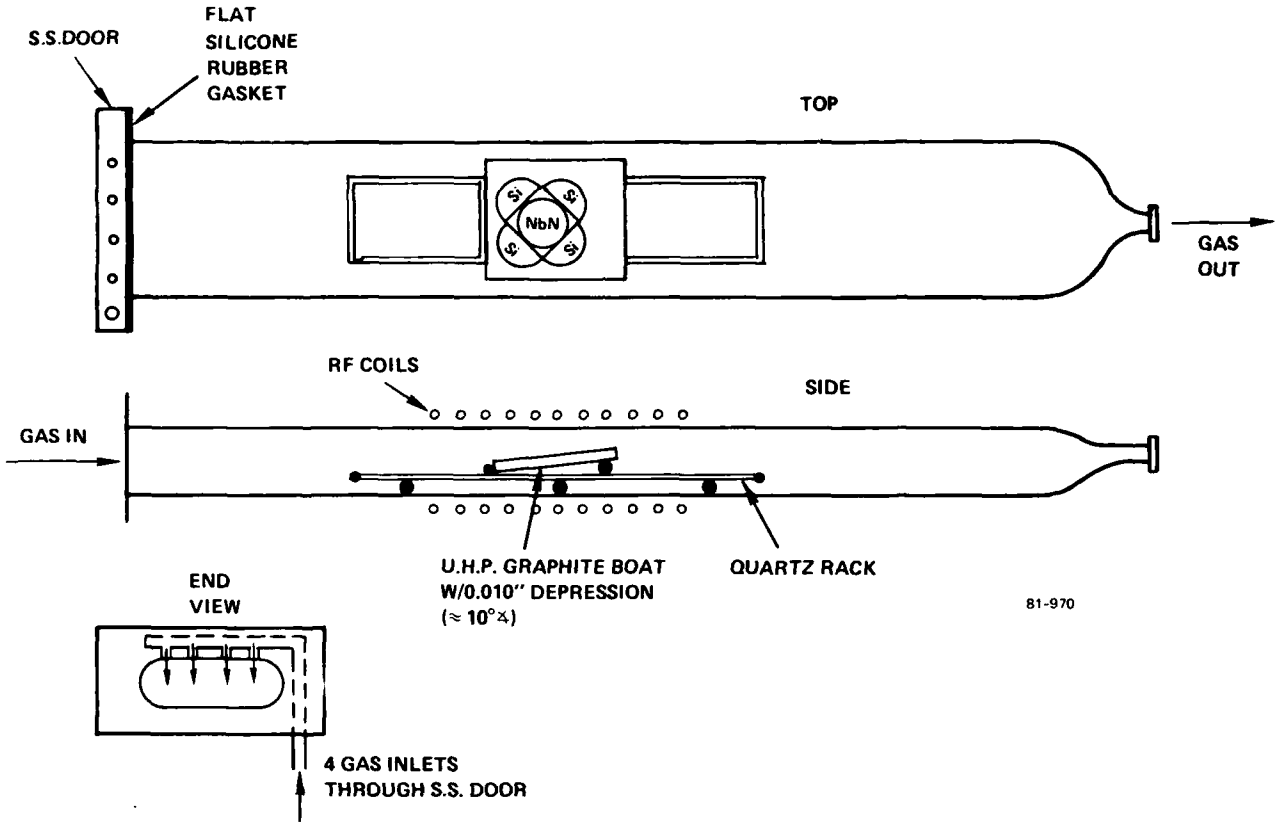

FIG. 4 Diagram of reactor used for chemical vapor deposition of silicon and germanium.

(1) The NbN layer was lightly sputter etched (100-150 Å of NbN was removed).

(2) The wafer was quickly transferred from the sputtering apparatus to the CVD reactor.

(3) Heating the wafer above room temperature began only after a flow of pure Ar was established.

(4) A mixture of Ar and NH_3 was used to anneal the wafer at 800°C for 15 minutes.

(5) A flow of pure Ar was again established and the temperature was reduced to the desired deposition temperature and the semiconductor barrier was deposited as soon as a stable temperature was achieved.

The NH_3 anneal was used both to remove any material which might have condensed on the wafer during transfer from the sputtering apparatus, and possibly to convert any niobium oxide which had formed during transfer to the reactor. The possible utility of the NH_3 anneal was suggested by Dr. M. Kestigian of SRC.

The NH_3 anneal did not change the T_c of even thin ($<$1000 Å) NbN layers. Annealing a pure Nb layer in such a manner converted the layer to NbN with a $T_c \gtrsim 10°K$. NbN layers produced by such an anneal had a different crystalline structure than did the NRL reactively sputtered layers as determined by x-ray diffraction. The NbN layers produced by annealing Nb were not at all suitable for device fabrication because they were extremely rough on a scale comparable to the thickness of possible barriers. The roughness was presumably due to the change in crystalline structure of Nb (cubic) and NbN (hexogonal + mixed cubic phases).

(2) "First Stage" Depositions. The CVD silicon layers used in the "first stage" were deposited at 725-760°C using techniques that were commonly in use for other research programs at SRC. The carrier gas was a mixture of 20% H_2 in Ar. The resulting layers were sometimes rough (indicated by a "haze" instead of being perfectly reflective).

(3) "Second Stage" Depositions. The occasionally observed rough layers prompted an investigation of the utility of the Si layer deposition process described by Taniguchi et al.[6] The group from Hiroshima University presented results on deposition of amorphous silicon layers by CVD at such low temperatures ($\approx 650^{\circ}C$) that amorphous silicon layers are expected. Our initial attraction to these amorphous silicon layers was the thought that grain size considerations might be irrelevant and therefore smoother layers of more uniform thickness might result. In addition the Hiroshima group reported both the highest conductivity, photoconductivity and sensitivity of electronic properties to doping of any previously reported experiments on amorphous silicon, including work on glow discharge Si-H alloys[7] and sputtered Si-H alloys.[8] Other attractions to this work included the sensitivity to doping of this material, which could perhaps be profitably used in adjusting properties of Josephson devices, and the fact that a relatively high deposition temperature was used, which might ensure that the barrier would not be disrupted by the subsequent high temperature deposition of the NbN counterelectrode.

Initial experiments confirmed many of the results of the Hiroshima group:

(1) Specular reflecting layers of high luster could be deposited.

(2) The growth rate was sensitive to the percentage of phosphorous incorporated into the layer by the addition of PH_3 to the silane, Ar and H_2 carrier gas.

(3) Extremely high conductivity and photosensitivity were observed.

However, the resistivity was so low ($\lesssim 10^{-3}\ \Omega$-cm) for heavily doped layers that we became suspicious that the layers were actually crystalline, not amorphous.

Two experiments confirmed this suspicion. First, undoped or boron doped layers (doped by the addition of B_2H_6 to the SiH_4 and carrier gas), which were much thicker (≈ 3000 Å) than the actual barriers, were found to be polycrystalline by x-ray diffraction. (W. Bekebrede of SRC undertook this analysis; heavily doped phosphorus layers grew at such a low rate that

layers thick enough for conventional x-ray diffraction studies could not be grown in a reasonable length of time.) Second, the heavily doped boron layers were electrically conductive at 4.2°K, indicating that they were degenerately doped. No previous observation of degenerately doped amorphous silicon has been reported - nor should it be expected.

The unexpected observation of polycrystalline silicon deposited at 650°C was a surprise to us and would presumably also be a surprise to the Hiroshima group. However, in this regard we should observe several differences between these present experiments and those performed earlier. First, we definitely observed polycrystalline and not amorphous growth only on Si_3N_4 or NbN substrates. Our previous experience that amorphous Si layers would be produced at such low temperatures was obtained from depositions onto silicon wafers with thermal SiO_2 coatings; the Hiroshima group used quartz substrates. The most definitive test we obtained for crystalline rather than amorphous silicon layers was obtained on p^+ layers, which were doped presumably near the limit of solid solubility of boron. Neither the Hiroshima group nor our previous experience encompassed such ranges of deposition parameters.

Experiments were conducted to determine the optimum deposition temperature for these low-temperature crystalline layers. Judging solely on the basis of luster (high reflectivity) a temperature of 675-680°C was chosen.

Investigations then began on the utility of employing unusually low temperature deposition of germanium. It was found that 380°C produced high luster Ge layers. (This was at a low enough temperature that we would a priori not have expected crystalline Ge.) As with the case for silicon, we confirmed polycrystalline layers by x-ray diffraction for the thicker layers (undoped or p^+). Again, it was observed that the addition of phosphorus by PH_3 to the germane severely reduced the growth rate at higher concentrations in analogy with the results obtained by the Hiroshima group on silicon layers.

The resistivity of the heavily doped germanium layer was within a factor of three of that which one would expect for epitaxial single-crystal germanium of comparable doping under the assumption that boron atoms are incorporated into the layer in proportion to their ratio to the concentration of GeH_4 introduced into the reactor. Reflectivities of these layers were measured in the infrared. The plasma resonances were relatively washed out compared to that of single crystal germanium. However, the wavelength of minimum reflectivity indicated boron doping of $\approx 8 \times 10^{19}$, for the most heavily doped layers.[9]

A summary of the properties of silicon and germanium layers which have produced in some sense "interesting" device properties is displayed in Table 1. Most recent experiments have used germanium more than silicon because of the expectation that the lower temperatures required might reduce chemical reactions between the semiconductor and the NbN. The lower semiconducting bandgap of germanium might also be expected to increase the tunneling current above that of silicon.[10]

Table 1. Summary of Si and Ge depositions used as barriers in NbN-S-Nb devices.

Barrier	Deposition Temperature (°C)	Dopant	Growth Rate (Å/min)	Resistivity (Ω-cm)
Si	760	B_2H_6	1500	10^{-3}
Si	760	PH_3	600	10^{-2}
Si	680	B_2H_6	1000	$10^{-1} - 10^{-2}$
Si	680	PH_3	250	$10^{-1} - 1$
Ge	375	AsH_3	50	10
Ge	375	B_2H_6	500	10^{-3}

(4) "Third Stage" Depositions. The "third stage" depositions were, unlike the earlier depositions, sputter deposited Si layers and not CVD layers. As mentioned above, the purpose of these experiments was

explicitedly to make contact with our highly reproducible Nb-Si-Nb SNAP technology. Because of our desire to emulate as completely as possible the Nb-Si-Nb technology, we chose to use, as closely as was possible, the current "best" technology.

The "best" technology went beyond that described in the first SNAP publication.[4] In order to ensure reproducibility by "uncomplicating" the processing, we had then been using undoped, unalloyed Si barriers, at the possible expense of producing higher capacitance devices. Since this was our current "most reproducible" Nb-Si-Nb technology, it was also incorporated into the NbN-Si-Nb devices.

Besides this change from Si-H alloy barriers, there was no other variation from the deposition techniques previously described,[4] except one whose significance we do not understand in any detail. In the original SNAP publication the deposition of the Si barrier immediately followed the deposition of the Nb lower electrode. In the current NbN program it was viewed that this was not only impossible (the NbN layers were deposited in Washington, DC and the barrier was deposited in Sudbury, MA), but undersirable. Therefore, a short sputter-etch ($\approx$100 Å of NbN removed) was used before the Si barrier was deposited. The sputter etch of the NbN could conceivably lower device quality. Keith and Lesley[11] have reported that Ar sputter etching a Nb foil can affect the properties of tunnel junctions subsequently formed on its surface.

The Si sputter depositions were performed in a PE2400 system, equipped with an oil diffusion pump. Background pressures below 10^{-7} T were obtained. For about two hours immediately before barrier depositions were performed, the system was also pumped with an auxiliary titanium sublimator to reduce the oxygen background. Occasional analysis of the residual gases in the system by an RGA (residual gas analyzer) showed a low hydrocarbon content, probably because of careful use of the system.

C. Thermal Oxidization of Deposited Barriers and Barrier "Cleanup."

Following barrier deposition the wafer was oxidized to "plug

pinholes." In the case of CVD barriers this was sometimes performed in situ in the reactor by first flushing out the reacting gases with argon and then introducing a pure oxygen gas. The oxidation was performed at 400°C for 10 min. For some CVD barriers a hot plate oxidization at 150°C for 30 min. using dry O_2 was used instead. We did not observe any obvious difference in device properties between these treatments. All sputtered barriers were given a 150°C hot plate oxidization.

All "stage two" and "stage three" barriers were lightly sputter cleaned in an Ar plasma[12,13] before deposition of a Nb counterelectrode. No sputter cleaning of the barrier was performed before deposition of a NbN counterelectrode.

D. Isolation by Anodization and Oxidation.

(1) Anodizing NbN Layers. As mentioned above, anodizing NbN layers is difficult and in general not satisfactory for the isolation of NbN devices in analogy to the SNAP procedure. Two anodizing solutions were tried: a concentrated solution of boric acid in H_2O[14] and a mixture of 156-g ammonium penaborate, 1120 ml ethylene glycol and 760 ml H_2O.[15] The anodized NbN layers tend to have uniform bright interference colors only if anodized to 10-20 V which produces an oxide that is too thin for effective isolation. Higher voltages applied to the anodization cell produce speckled layers of various colors that are mechanically weak. The anodization presumably proceeds preferentially along grain boundaries.[16]

Occasionally we have anodized NbN layers to 35-50 V using the ammonium pentaborate electrolyte and have obtained smooth, continuous oxide films. However, in removing photoresist used to mark active device areas with acetone, the oxide film broke up and became speckled. The disruption of the film proceeded slowly enough across the wafer that a "wave front" of disruption would often be observed to move across the wafer. Complete disruption took 10 s to 10 min.

Even if the NbN anodization resulted in an oxide of suitable quality, one could not use the technique[4] of monitoring cell voltage as a

function of time with constant current source to monitor the complete anodization of the upper NbN film. With a Nb upper electrode, this procedure results in a change in slope of V vs time when the upper electrode is completely anodized.[4] As shown in Fig. 5, the voltage as a function of time for the anodization of a simple NbN layer (no underlying barrier) is a complicated and poorly understood shape. This shape is generally not reproducible.

Anodization of a Nb upper electrode is generally useful for devices which have a NbN lower electrode. With a sputtered silicon barrier there is a change in slope at a voltage V_B, which marks the complete consumption of the upper Nb film. As illustrated in Fig. 5, qualitatively, we obtain the same results as for a Nb-Si-Nb device.[4]

With CVD polycrystalline barriers, a well defined change in slope is also obtained with a Nb upper electrode and this is sufficient for determining when the Nb is completely consumed. However, if one continues to anodize beyond V_B by more than about 10 V, peculiarities are sometimes observed with poly-Ge barriers. Sometimes there is a second change in slope, as illustrated in Fig. 5, whose significance we do not understand. Once we accidentally continued the anodization to 30 V beyond V_B. The V vs time curve became "noisy" and a disruption of the anodized film and barrier occurred. A tracing of this particular V vs time is also included in Fig. 5.

(2) Oxidizing NbN Layers. Isolation of devices by thermal oxidation of the upper NbN electrode was also studied. About 250 Å of NbN is converted to an oxide after heating the wafer in pure O_2 at 400° C for one hour. The rate of oxidization seems to vary slightly with different NbN layers. Many NbN layers can be oxidized to yield a uniformly high reflectance oxide layer. A few show evidence of preferential oxidation about some grain boundaries. However, even with these layers, a much more rugged and uniform oxide is produced than could be obtained by anodization.

Thermal oxidation does not provide an in-process method of determining the complete oxidation of the layer as does Nb anodization. We

have attempted to provide a partial check for this by first oxidizing a small piece of the wafer and observing when the oxide color stops changing time and then using at least that length of time to oxidize the rest of the wafer. This method is capable of error, however, because the interference colors are also affected by the thickness of the very thin barrier underneath. Unfortunately, our "best" oxidization was achieved on an upper NbN layer which had only a T_c = 9.5K.

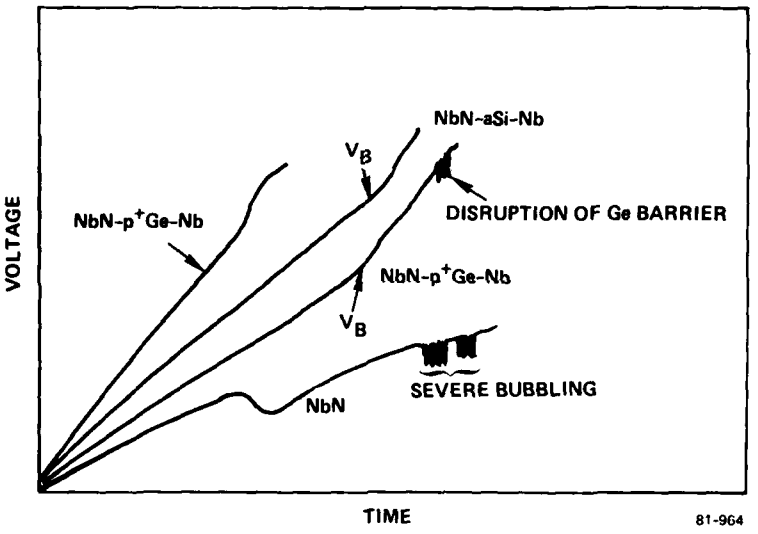

FIG. 5 Anodization cell voltage as a function of time for four different wafers with arbitrary scales. The change in slope at V_B signifies the complete anodization of the upper electrode. Other structures are poorly understood (see text). The NbN curve was obtained from a single NbN layer (no barrier underneath).

SECTION III

RESULTS

This section is divided into four parts. In Part A we comment briefly on our "first-generation" NbN devices. CVD deposited Ge barrier devices are covered in Sec. B, and sputtered Si barrier devices in Sec. C. Section D discusses NbN counterelectrode devices, the previous devices all having Nb counterelectrodes. Section D tends to be somewhat speculative since successful all-NbN devices have just been successfully fabricated.

Table II includes basic results on the three major barrier types and all reasonably successful fabrications. Under I-V type we use the term "tunnelling" or "weak link." "Tunnelling" type I-V's are patterned after the classic BCS curve with high resistance below the sum of the superconducting energy gaps of the two electrodes, and a sharp increase in current at this sum. Also implicit in this description is a large amount of hysteresis ($\rho < 1$). "Weak link" refers to a device with roughly linear I-V characteristics and little or no hysteresis. No features are seen at the sum of the energy gaps. Specific I-V curves presented throughout this section will help understand our use of these terms.

A. "First Stage" Devices

The first NbN-poly Si-Nb and NbN-poly Si-NbN devices fabricated before and just after this program began served more as an existence theorem that deposited barriers could be used with NbN electrodes than evidence of particular ideal I-V characteristics. These devices had $I_c R_N < 0.1$ mV with weak link characteristics. Nevertheless, they were Josephson devices: Shapiro steps were observed at NRL and nonideal threshold curves were observed at SRC. Figure 6 displays a threshold curve observed on a NbN-Si-Nb device.

B. CVD Ge Barrier Devices

(1) Arsenic-doped (type n) barriers. The initial run using this barrier (7/22/80) resulted in weak link type devices with large critical

TABLE II
NbN FABRICATION RESULTS SUMMARY

DEVICE	NN (RUN #)	NN T_c	I-V TYPE	I_cR (mV)	R*	MODULATE		COMMENTS
Ge - p^+ CVD								
4/7/81 A	$156a_1$		Schottky	-	1 - 20 Ω			
5/4/81 A & B	156b		Schottky	-	½ - 10 Ω			A HF before Ge, B sputter etch.
5/6/81 A & B	158		Schottky	-	½ - 10 Ω			A sputter etch, B HF before Ge. Known bad NbN run, heater failed.
5/19/81 A	$156a_2$		Weak Link	Low		OK		
6/3/81 A	158		Weak Link	Tiny		OK		Known bad NbN run, heater failed.
8/12/81 A	165	11	Weak Link	0.01 - 0.1		~ 90% Irregular		
Ge - n CVD								
10/16/80 A	134		Tunneling – Δ Low	~ .7	.1 - 5 Ω	Good		R subgap > R above gap, sum Δ's = 1.5 mV.
12/10/80 A	138A		Tunneling	~ .4 - .8	2 - 20 Ω Some higher	Good		Very low V_m, sum Δ's = 3.4 mV.
1/5/81 A	138C		Tunneling – Δ Low	~ .01 - .1	.05 - .2	OK		Low V_m, sum Δ's = 1 mV.
8/13/81 A	165	11	Weak Link	~ .01 - .1	.01 - .1	Fair		Curves concave down, no gap structure.
Sputtered α - Si								
2/14/81 A_3	70		Tunneling	~ .7	20 - 200 Ω	Good	84 Sec. Si	Low current density, sum Δ's = 3 mV.
5/20/81 A	156C		Tunneling	~ 1	5 - 10 Ω	Good		Vm to 15 mV, best devices.
6/4/81 A	158		Tunneling, Δ Low	.2 - .4 mV	10 - 200 Ω	Good		Low Vm. Known bad NbN run, heater failed.
8/6/81A	165	11	Weak Link	~ .1	.01 - .1	Poor		
8/6/81 B	176	13	Tunneling, Δ Low	~ .4	.005 - .02	OK		Sum Δ's = 2 mV.

*Device areas range from about 100 μ^2 to 1000 μ^2. Many of the devices are of such poor quality or uniformity that this number can be thought of somewhat qualitatively.

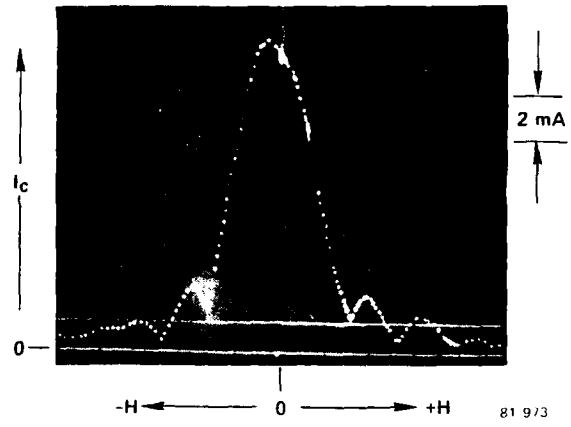

FIG. 6 Threshold curve for a first-generation NbN-aSi-Nb device.

currents (10's mA). 9/22/80A on NN-46 again yielded overly large critical currents. Finally, 10/16/80A on NN-134 yielded reasonable critical currents on devices that had a tunneling type I-V characteristic (see Fig. 7(a)). The sum of the energy gaps was much smaller than expected. This has tentatively been ascribed to poor surface condition of the NbN lower electrode, and is discussed more fully in Sec. C. 12/10/80A was a slightly longer Ge deposition than 10/16/80A and resulted in relatively nice devices. The main problem with these devices was that the observed $V_m \lesssim 1$ mV was very low. However, the observation of the sum of the gaps at 3.4 mV constitutes an existence theorem that the arsenic doped CVD process used in the fabrication does not in itself lower the energy gap at the NbN surface.

Run 1/5/81A on NN-138C was essentially a repeat of 10/16/80A. The resultant devices displayed the low gap syndrome, as seen in Fig. 7(b). In general, they had little hysteresis, and some looked very weak linkish.

The most recent fabrication was 8/13/81A which was again an attempted repeat of 10/16/80A. This time the NbN lower electrode was of known poor quality (NN-165, T_c = 11 K), and the resultant devices were uniformly poor (see Fig. 8(b)). Note that what is presently considered poor would have been very encouraging when this work was begun in late 1979. The measured thickness of "interesting" n-Ge barriers was in the range of 45-55 Å.

(2) Boron-doped (type p^+) barriers. The first p^+ CVD polycrystalline barrier device attempted was 3/11/81A on NN-153. The Nb counterelectrode on this wafer failed during anodization and the resultant devices all looked like shorts. Similarly with 3/27/81B on NN-152.

Following this was 4/7/81A, 5/4/81A and B, and 5/6/81A and B on NN-156a, NN-156b and NN-158a, respectively. These barriers varied somewhat in thickness and doping concentration, but were remarkably uniform and reproducible. They all had super-Schottky-type I-V characteristics with resistances in the range of 1/2 - 10 Ω. This is seen in Fig. 9(a). Barrier thickness was $\lesssim$130 Å.

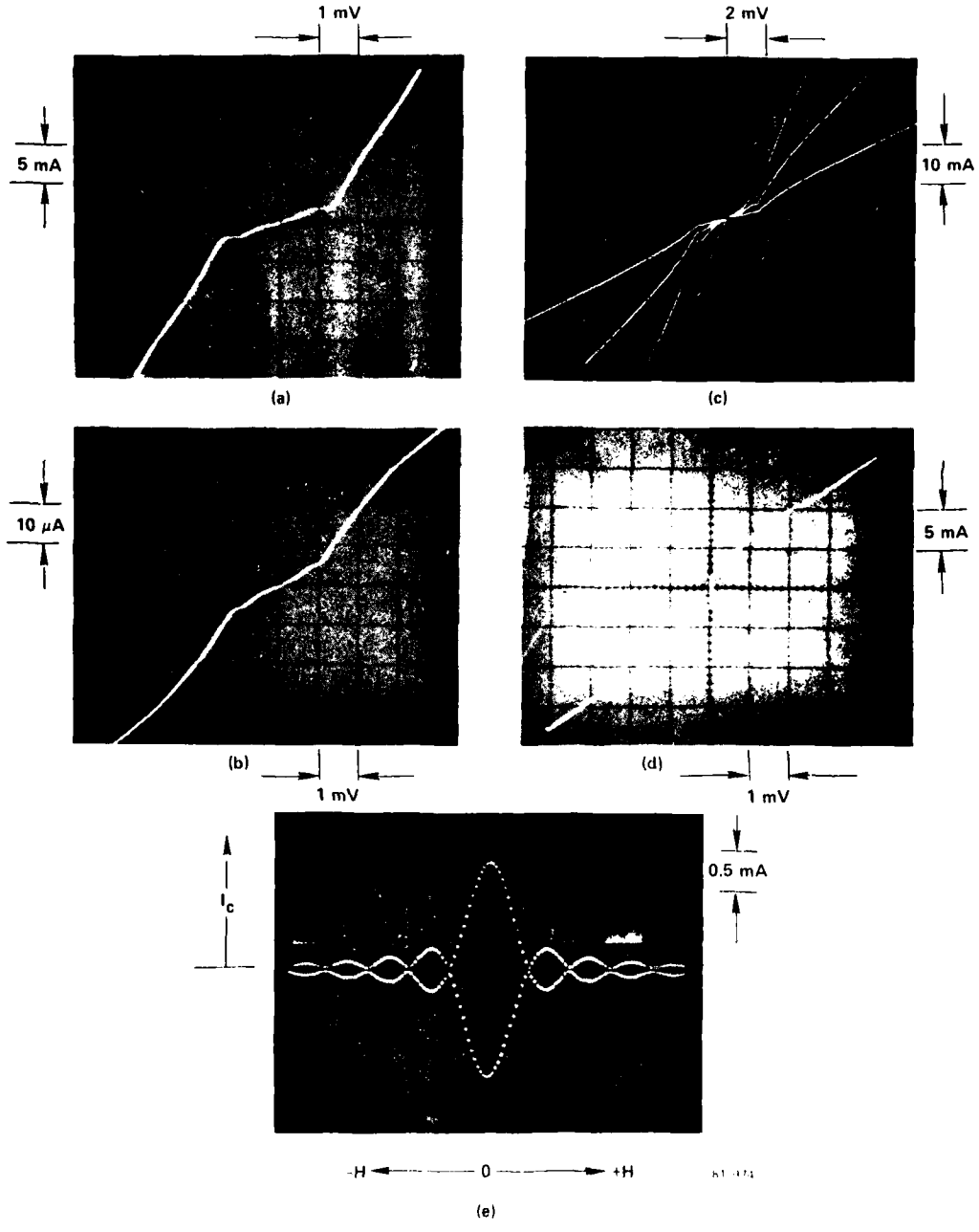

FIG. 7 Characteristics and threshold curve for several low gap NbN–semiconductor Nb devices:

(a) I-V for n type Ge (10/16/80A)
(b) I-V for n type Ge (1/5/81A)
(c) I-V for a Si (6/4/81A)
(d) I-V for a Si (8/6/81A)
(e) Threshold curve for n type Ge (10/16/80A).

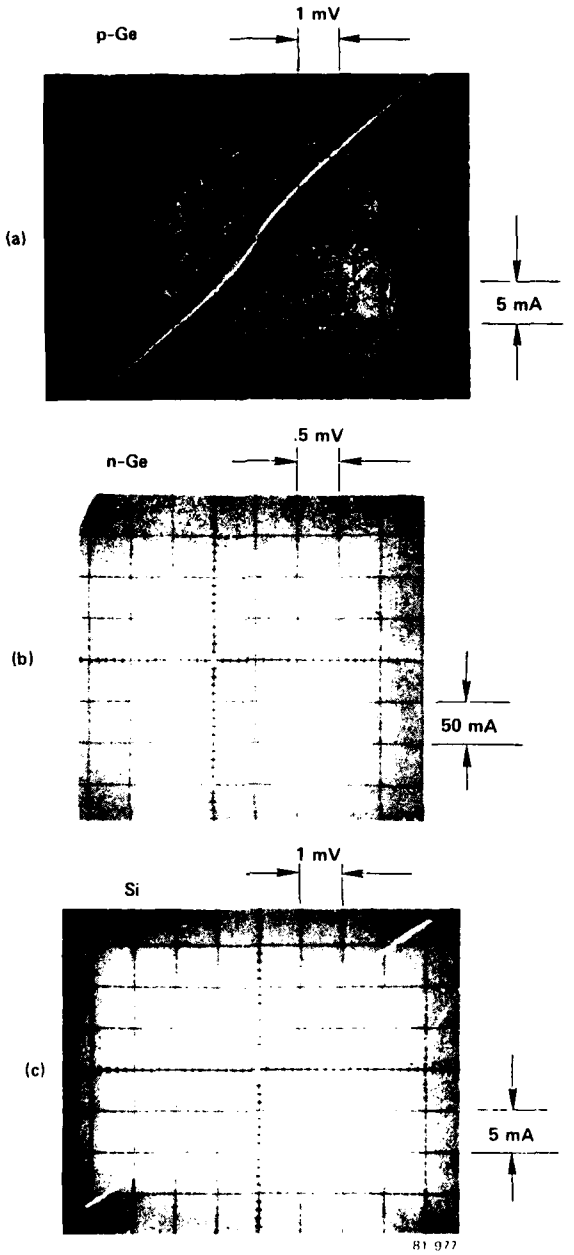

FIG. 8 I-V characteristics for:

(a) p^+ Ge barrier on NN165

(b) n Ge barrier on NN165

(c) a Si barrier on NN176.

NN165 has T_C = 11 K and NN176 has T_C = 13 K. All devices have modulable critical current.

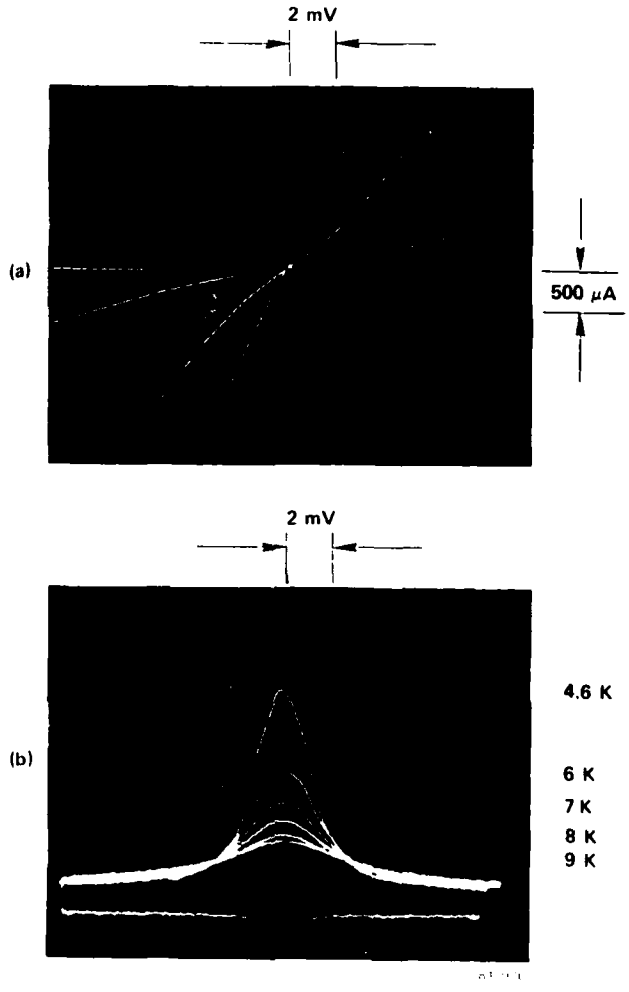

FIG. 9 Super-Schottky characteristics for NbN-p^+ Ge-Nb devices.

(a) I-V characteristics for several devices – device conduction scales with area.

(b) $\frac{dV}{dI}$ vs. V for device C (sample is 5/6/81B, chip B3). Different curves represent data taken at 4.6, 6, 7, 8 and 9K (with highest $\frac{dV}{dI}$ obtained at lowest temperature).

Attempts to produce thinner barriers and observe Josephson current were made on 5/19/81A with NN-156a$_2$ and 6/3/81A with NN158. These devices had relatively large current densities, but the I-V characteristics tended to look like weak links. A fabrication on NN165 with T_c = 11 K (8/12/81A) yielded similar results, as shown in Fig. 8(a).

From the above results we propose the band diagram shown in Fig. 10. The NbN forms a Schottky barrier with the p^+ Ge, while the Nb forms an ohmic contact. We will elaborate further upon the implications of this in Sec. III D.

The super-Schottky devices are interesting in their own right. One of the major disadvantages of most earlier super Schottkys is the large impedance of the semiconductor side of the device.[17] (An exception is the silicon membrane structures of Huang and Van Duzer.[2]) In our devices this impedance is minimized by the ohmic contact to the Ge barrier of the superconducting Nb counterelectrode. Figure 9(b) shows dV/dI vs V for one of these devices at various temperatures, and Fig. 11 shows a more detailed plot of dV/dI taken at V = 0 as a function of temperature. This is replotted as ℓn dV/dI vs 1/T in Fig. 12. From the slope of the curve we infer an activation energy of 0.9 mV. As can be seen, these devices have significant nonlinearity up to 9K, and there is no break in the ℓn dV/dI curve near the T_c of Nb. This latter point tends to confirm that it is the NbN-Ge Schottky barrier which is the major contributor to device impedance.

From the room-temperature resistivity measurements on thicker layers which were deposited in the same manner, we would infer a doping density of the order of $N = 3 \times 10^{19}/cm^{-3}$, assuming the same mobility as for single crystal Ge. A zero-bias depletion width W for such a layer, which makes a Schottky contact to metal which produces, say, 0.3 V "built-in" voltage V_{bi} is given by

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{q N}} \approx 40 \text{ Å} \quad .$$

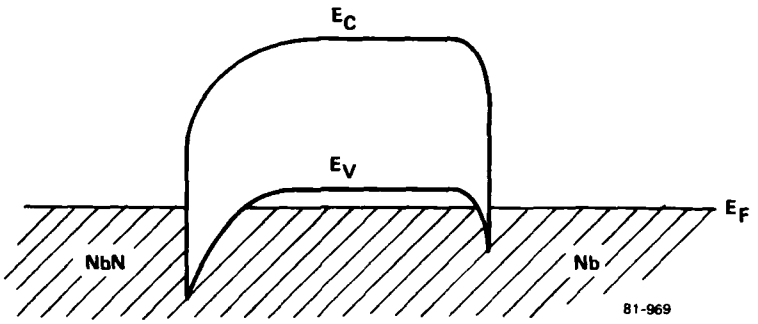

FIG. 10 Proposed band diagram for NbN-p^+Ge-Nb device.

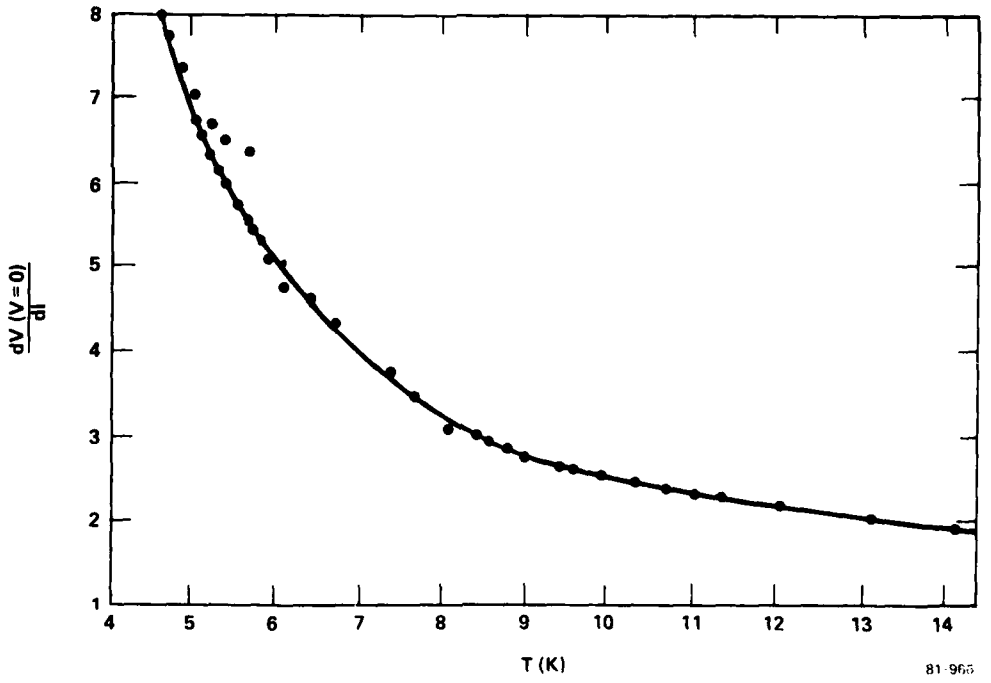

FIG. 11 A plot of $\frac{dV}{dI}$ at V = 0 vs temperature for NbN-p^+Ge-Nb device (5/6/81A, chip D6, device C).

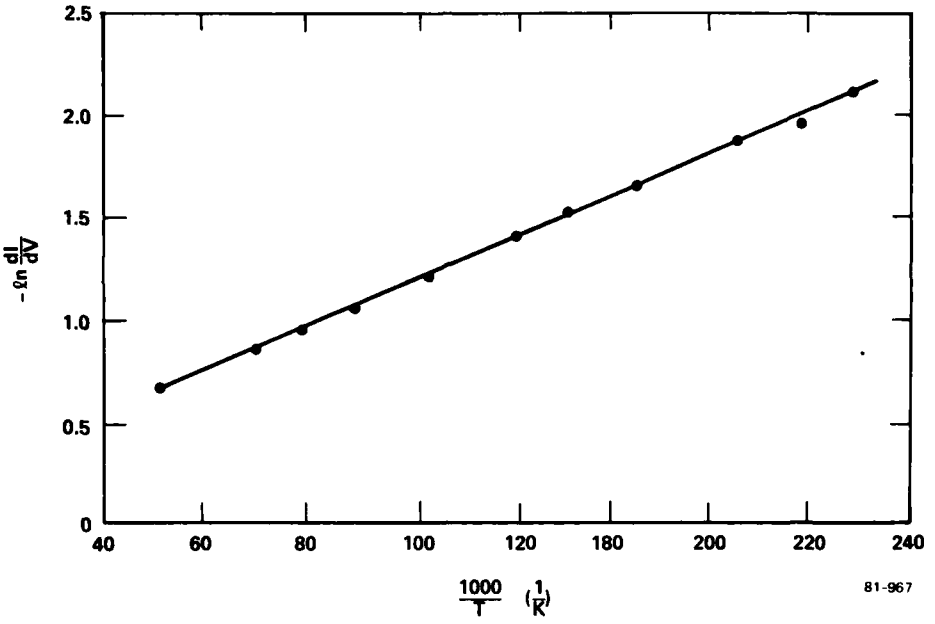

FIG. 12 A plot of $-\ell n (\frac{dI}{dV})$ as a function of $\frac{1000}{T}$ for the data of Fig. 11.

This is less than the thickness of the deposited layers and provides very rough corroboration of the interpretation that there is a region of undepleted Ge with "normal metal" characteristics between the NbN Schottky and the Nb contact.

C. Si Barrier Devices

Early attempts at using a silicon barrier employed CVD silicon and conventional junction formation, that is, deposition of the barrier through an insulator window. These results have already been discussed in Sec. III A. The first attempt to use a Si barrier in a SNAP processed device was 6/18/80 A & B. These used αSi deposited in our older Cooke sputtering system with hydrogen and phosphorus. The resultant devices had large supercurrents that did not modulate with magnetic field. This approach was abandoned as nonproductive.

The next attempt to use a Si barrier was 2/14/81 A_3 and B_3. This attempt followed the successful development of Nb based SNAP processed tunnel junctions using Si sputtered in the Perkin-Elmer 2400-8SA system. No hydrogen or dopant was used for these barrier depositions. Two wafers were processed, NN70 and a niobium wafer. The Si deposition was 84 sec long. The intent was to make contact to the "standard" niobium process. The result on the niobium base electrode was devices with good V_m, $I_c R \sim 1$ mV and resistances of a few ohms. The NbN base electrode devices also had fairly good quasiparticle characteristics, as can be seen in Fig. 13. The product of the critical current and the device normal resistance $I_c R$ was also good (as nearly as could be determined), since the resistance of these devices was very high, on the order of 100's of ohms, thus making the critical current nearly unobservable. The sum of the gaps was about 3 mV, which is not quite as high as it should be. The conclusion we drew from this result was that the NbN-Si interface has a higher barrier height than the Nb-Si interface, thus a thinner Si barrier would be necessary to achieve reasonable current density. Also, the quality of the quasiparticle characteristic was the best to date on a NbN electrode-based device.

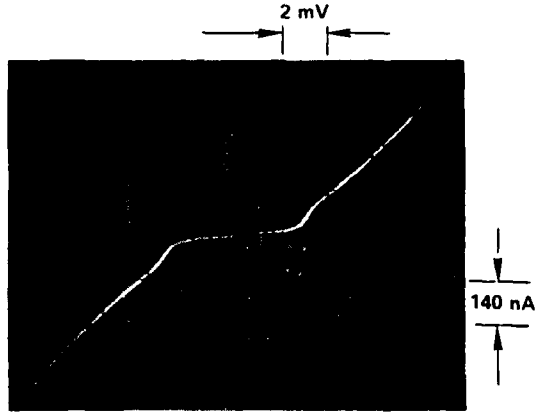

FIG. 13 I-V characteristics of first successful a Si barrier device (device C, chip #7, of 2/14/81A). No supercurrent is visible because of high resistance.

The effect of the NbN on raising the barrier height was substantiated by an earlier experiment (11/25/80) in which a Nb-Si barrier device received about 50 Å of niobium reactively sputtered in nitrogen in the 2400-8SA system at ambient temperature. The devices then received regular niobium and were completed using the SNAP process. The resultant devices had good quasi-particle characteristics but the resistance was substantially higher than devices having the same barrier, but receiving the standard niobium counter-electrode. Thus, we feel that to first order the barrier in a NbN-αSi-Nb tunnelling device can be represented as shown in Fig. 14.

The next attempt was with a 66 sec Si deposition. Problems were encountered during the wet etch of the contact niobium layer, during which some of the devices literally fell apart. The characteristics of the resultant devices ranged from shorts, through super-Schottky-type curves to some high resistance weak link type devices. The results were ambiguous but were interpreted to indicate that a yet thinner barrier was required to achieve a resonable current density. 36 sec was chosen for the subsequent run (5/20/81A) on NN156C. This run yielded the result shown in Fig. 15. I_cR was about 1 mV, V_m up to 15 mV and the sum of the gaps was $\sim$3.5 mV. Except for the fact that the time of the Si deposition was 43% of the time of a niobium-based device, this process is essentially identical to our standard SNAP process. Thus, we expect the barrier and upper interface to be quite reproducible and uniform.

Figure 16 shows a plot of the peaks in the dV/dI curve for a device on 5/20/81A as a function of temperature. Typically, the value of the energy gap is identified with the minima in dV/dI (conductance peaks), however, the dV/dI maxima are sharper over the full temperature range, and hence were plotted. Thus, the identification of these points with the energy gap is not to be taken literally. The point of this plot is that it is reasonable to infer that these structures can be identified with the sum and difference of the Nb and NbN energy gaps in terms of their temperature dependence. The temperature values used to fit the data are T_c = 14 K for NbN and T_c = 9.2 K for Nb. These are quite reasonable. Shown in Fig. 17

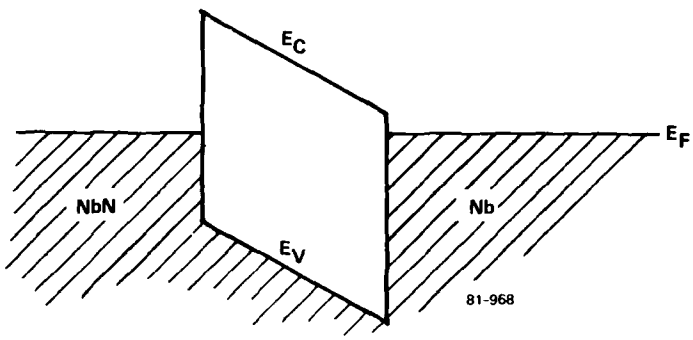

FIG. 14 A proposed band diagram for NbN-a Si-Nb device.

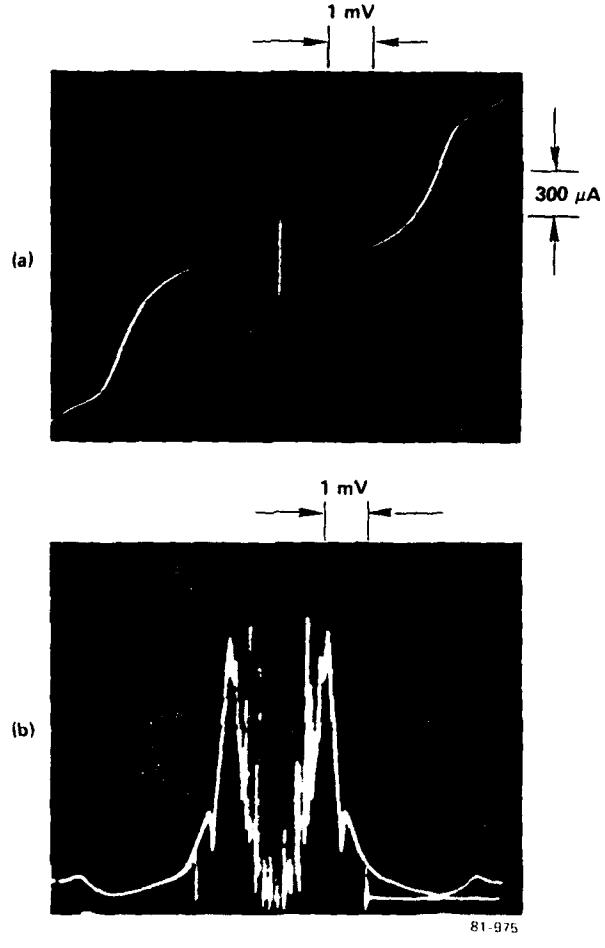

FIG. 15 I-V and $\frac{dV}{dI}$ vs V characteristics at 4.2 K for NbN-a Si-Nb device (device D, chip #7, 5/20/81A):

(a) I-V characteristics

(b) $\frac{dV}{dI}$ vs V.

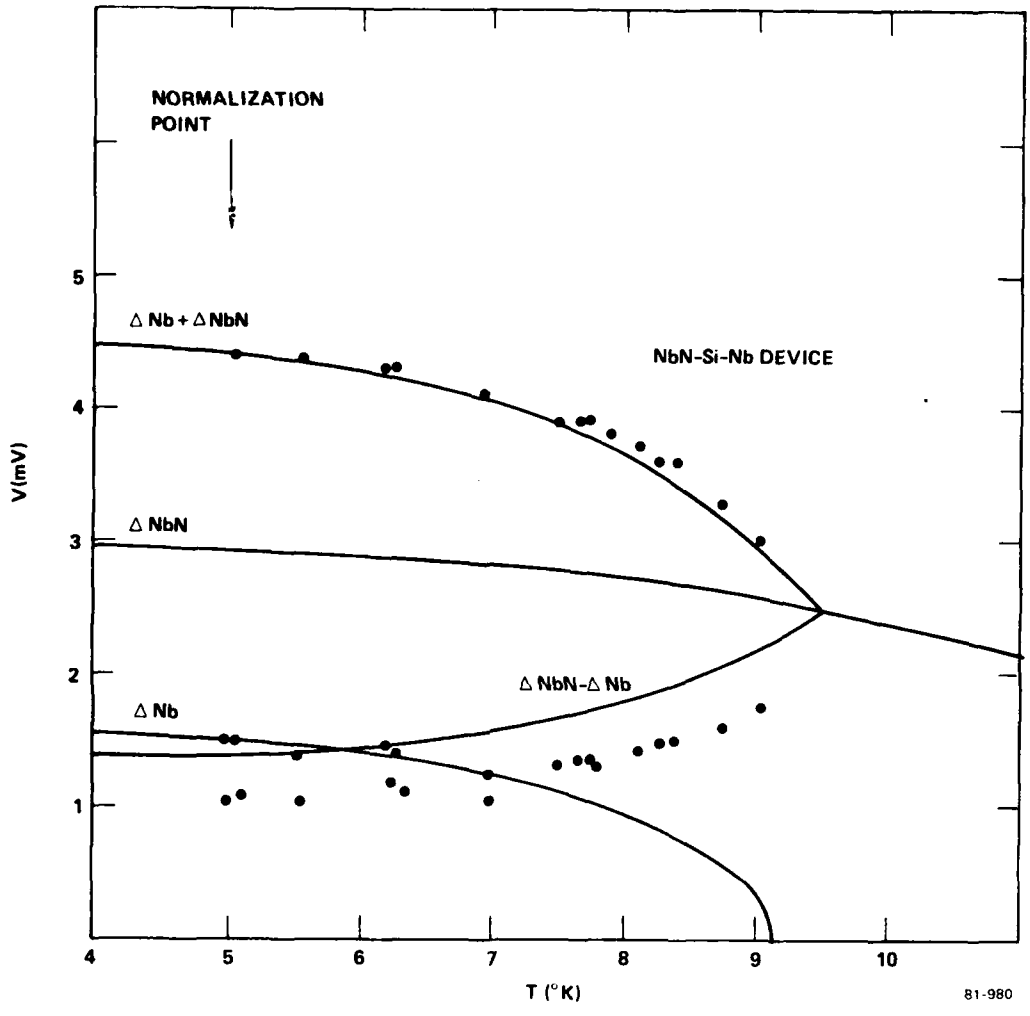

FIG. 16 A plot of peaks in $\frac{dV}{dI}$ vs V as a function of temperature for NbN-a Si-Nb device whose I-V is shown in Fig. 15.

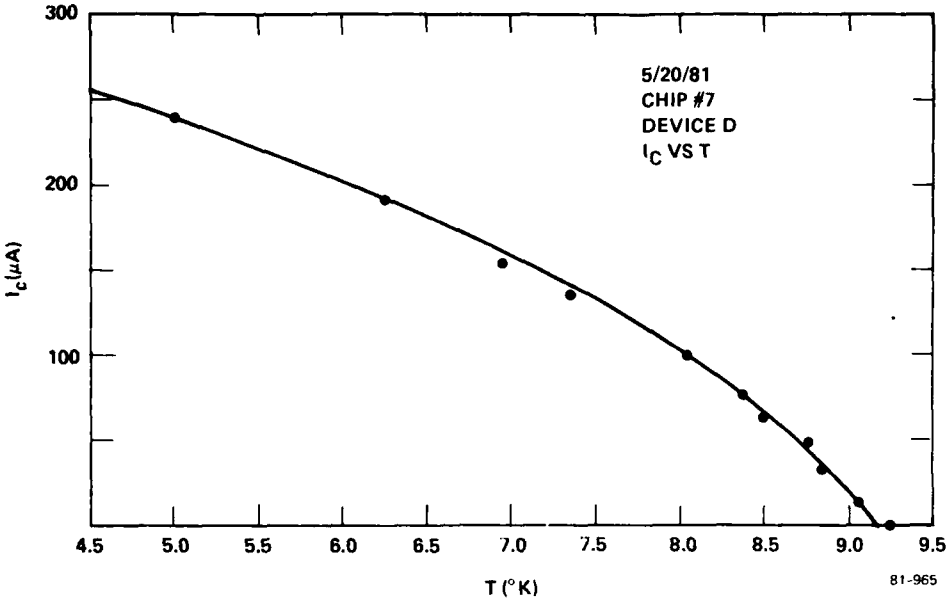

FIG. 17 Critical current as a function of temperature for a NbN-a Si-Nb device.

is a plot of I_c vs T for one of these devices. Again, the result is just what would be expected for a tunnel junction with Nb and NbN electrodes.

We have studied the low voltage resonances of one of these junctions (these resonances are not visible in Fig. 15(a)), and compared the results with similar resonances on all-Nb, Si barrier junctions. If we assume that the dielectric constant is the same in the a-Si barrier regardless of the lower electrode material, we infer that the thickness of the barrier in the NbN devices is 43% of the thickness of the barrier in our "standard" Nb devices. The deposition time of 36 sec, fortuitously enough, is 43% of the 84 sec standard Nb barrier deposition! Due to the large parasitic capacitance associated with the geometry of these structures we choose not to infer an actual capacitance from this data. However, from data on Nb- Si-Nb devices that were designed to measure capacitance made using another mask set, we have found a specific capacitance of 0.025 pF/μm^2. If we use the ratio of NbN-barrier thickness to Nb barrier thickness with this value, we find a specific capacitance of 5.8 pF/100 μm^2. This is slightly higher than for Pb alloy junctions.

The next fabrication was 6/4/81A on NN158 using 33 sec Si deposition. This curve is shown in Fig. 7(c) and is a very important result. Qualitatively, the I-V characteristic is the same as for devices 10/16/80A and 1/5/81A (Fig. 7(a) and (b)), but these latter devices were fabricated using n-Ge barriers. All of these devices have a subgap resistance that is higher than the above gap resistance. Also, the gap is anomalously low. It is possible to interpret this as being due to the surface of the NbN being contaminated or structurally deficient. The structure observed is the Nb gap plus and minus a small contribution from the NbN. Subsequently, it was determined that the substrate heater went out some time during the deposition of NN158. The evidence on NN134 and NN138C is less clear cut.

In order to test the effect of the NbN quality on junction characteristics, two NbN samples, NN165 (8/6/81A) with T_c = 11K and NN176 (8/6/81B) with T_c = 13.3 K were processed using 33 sec Si barriers deposited at the same time. The resistance of these devices was lower than previous

silicon runs due to the fact that the wafers were located off center during the deposition, thus receiving slightly thinner Si barriers. I_cR for NN165 was typically 0.2 mV or less, while NN176 resulted in I_cR = 0.5 - 1 mV. Gap structure was not observable on NN165 but was found on NN176 at a sum of 2 mV. This is shown in Fig. 7(d). Overall device quality is not good, but the modulation of the critical current with magnetic field indicates that the devices are fairly uniform. p^+-Ge barriers were fabricated on two additional wafers with NN165 (Figs. 8(a) and (b)). These devices were also poor, with no visible gap structure and weak link type I-V characteristics.

More recently, a group of NbN wafers of widely varying quality was received. One film was not superconducting at 4.2K, while the best had T_c = 15 K. It was decided to measure the reflectance of these films as a function of wavelength in order to see if there might be any correlation with T_c and/or tunneling data. The results are shown in Fig. 18. In general, the films with the highest T_c were the most reflective. Also, the films that were anomalous (not superconducting, broad transition) have a reflectometry trace with a quite different slope from the others.

Four of these films have just undergone processing with identical Si barriers to correlate the junction characteristics with the optical and T_c data. These experiments have been just completed (and these very preliminary results represent more a "note added in proof" than a well-thought-out interpretation). Nevertheless, these preliminary results may be significant. It should be noted that:

(1) Except for the NbN deposition, all wafers were processed simultaneously (and therefore identically).

(2) The silicon-barrier deposition procedure was identical (except for thickness and the NbN sputter etch) to our highly reproducible Nb-Si-Nb SNAP.

On the other hand the fabricated devices were different:

(1) Devices on any one wafer were essentially similar with regard to the shape of their I-V characteristics.

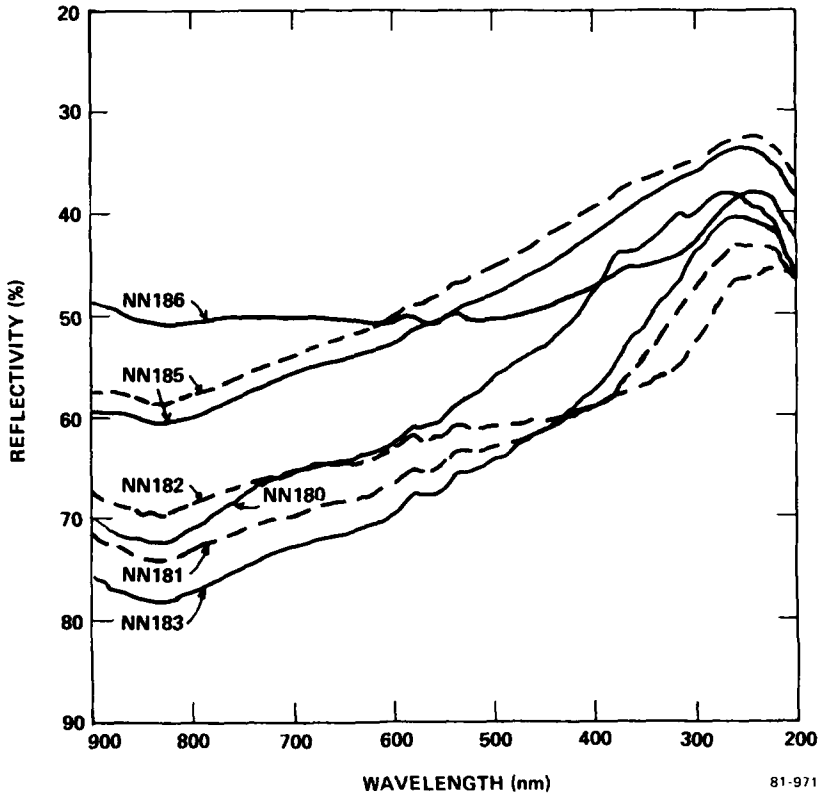

FIG. 18 Reflectivity vs wavelength for six different NbN films. NN185 has a broad transition from 10–16 K, NN182 is not superconducting at 4.2 K, NN180 has T_C = 12 K, NN181 has T_C = 14.8 K, and NN183 has T_C = 15.2 K. NN186 is a thin NbN film on top of a NbN–p^+ Ge sample. The two curves for this sample are at opposite ends of the wafer.

(2) Devices on different wafers were different from each other.

(3) Devices with good tunnelling characteristics from different wafers had the same normal resistance. This last observation reinforced our confidence that the silicon barrier is reproducible over the entire group of wafers.

Additional work will be necessary to fully correlate junction characteristics with T_c and with reflectometry. It may even be possible that reflectometry may have more power than measurements of T_c in predicting good quality tunnel junctions. At the least, these experiments show that the lower NbN electrode is critical in the determination of good tunnelling properties.

D. NbN Counterelectrode Devices

The ultimate goal of this work is to produce devices of "good" quality using NbN for both the upper and lower electrode. In order to achieve this, our approach has been to learn how to fabricate NbN-Nb devices and then turn to NbN counterelectrode devices. Thus a major portion of our effort has been directed at NbN-Nb devices; however, in most cases samples (usually half wafers) have been returned to NRL for NbN counterelectrode deposition. This transitory goal has been achieved; good NbN-Nb devices have been demonstrated. In addition, we are beginning to understand why some devices are of very poor quality. Since the effect of the NbN counterelectrode deposition on the devices' characteristics is unknown, we are pursuing three separate barrier types: p^+-Ge and n-Ge, both deposited using low temperature CVD, and resulting in polycrystalline films, and sputtered α-Si, which is deposited at relatively low (ambient) temperatures.

The NbN-Nb results using p^+-Ge seem to indicate that NbN forms a Schottky barrier with p^+-Ge and Nb forms an ohmic contact. This system would not be expected to form a good tunnel junction since the Nb-Ge interface would always tend to resemble a normal metal with a short mean free path and the attendant degradation of the Josephson current and energy gap. However, an all-NbN device with this barrier would be postulated to consist

of two back-to-back Schottky barriers. This should have excellent tunneling characteristics. The resistance of this device would be higher than that of the same NbN-Nb device according to this model, perhaps by one or more orders of magnitude. Thus, the thinner barriers such as 5/19/81A should provide the best prospects.

Both n-Ge and Si barriers have yielded devices with promising tunnelling I-V characteristics. It is known that NbN-Si has a higher barrier height than Nb-Si. The barrier height of NbN-nGe may be comparable to Nb-nGe and Nb- Si, since barrier thicknesses of 55-65 Å on NbN-nGe-Nb devices seem to yield device resistances comparable to barriers of similar thickness in Nb-Si-Nb devices.

The Si must be considered the most promising candidate since quite excellent Nb counterelectrode devices have been produced using this material. Also, we have extensive experience with sputtered Si barriers in all-niobium devices. It has been demonstrated (11/25/80A) that it is possible to successfully use this barrier with a NbN counterelectrode even though this counterelectrode was not deposited under conditions appropriate to producing high-quality NbN. The main cause for worry is the effect the high-temperature NbN deposition will have on this barrier. In this case, the higher temperature CVD Ge barriers may be posited to have a better chance of surviving.

Initial attempts to use anodization to isolate the junctions were a failure. Films of NbN can be anodized, but as the voltage increases the anodic oxide becomes progressively hazier and rougher. When the NbN is on top of a semiconductor barrier this problem is exacerbated. Subsequently, we have attempted to use thermal oxidation ($400^{\circ}C$ in O_2) to isolate the junctions, with SiO_2 being used as the masking material. Our most recent attempt to fabricate NbN-Ge-NbN by thermal oxidization succeeded in isolating the upper electrode and almost certainly in producing the desired devices. The devices were of the weak link variety but modulated well.

The reason for saying that the desired devices were "almost certainly" fabricated rather than "certainly" fabricated involves the fact that

the upper NbN electrode was deposited at ambient temperature (in order to be conservative in not disrupting the barrier) and therefore had a T_c of approximately 9.5K. The contact (wire) superconducting metal which connected the upper electrode to the pads was Nb with $T_c \lesssim 9K$. Therefore, one could argue that the observed I-V characteristics could have been due to the (unintentionally)formed JJ devices between the upper NbN electrode and the wire Nb. With a low critical current ($\lesssim$100 uA) at 4.2K, the supercurrent cannot be detected at $> 9K$. Therefore, one could argue that we cannot distinguish between an intentional NbN-Ge-NbN junction and an inadvertently formed NbN-?-Nb junction.

The latter possibility we view as improbable. First, other experiments have shown no difficulty in forming superconducting short circuit contacts between NbN and Nb, even if most of the area of the wafer was thermally oxidized NbN. (These contacts are made by sputter depositing Nb after lightly sputter etching the wafer.) Second, other experiments, including the deposition of Ge at greater than the oxidization temperature, showed that a supershort or high conductivity Josephson device is not produced by annealing Ge with NbN. We therefore assume that NbN-Ge-NbN devices have in fact been fabricated by the thermal oxidization variation of the SNAP procedure.

SECTION IV

SUMMARY AND CONCLUSIONS

The results of this program can be summarized as follows:

(1) NbN-aSi-Nb devices have been demonstrated with the highest V_m (= 15 mV) parameter (product of critical current and subgap resistance) of any reported all-refractory superconductor device.

(2) The "jump" in quasiparticle current for the NbN-Si-Nb device at the sum of the superconducting energy gaps is not as abrupt as theoretically predicted. This implies two obvious facts:

(a) The real devices have a much greater subgap leakage near the sum of band gaps than at lower voltages.

(b) These present devices will not behave as well as mm detectors as other S-I-S devices.

(3) NbN-p^+ Ge-Nb devices can result in low series resistance super-Schottky devices.

(4) NbN-Ge-NbN have probably been demonstrated in a structure in which the entire trilayer is formed before any patterning with isolation between devices provided by thermal oxidization of the upper NbN electrode.

(5) The semiconductor barriers used in these studies have a primary affect on device conductance, etc.; the quality of the superconducting tunnel junctions is determined primarily by NbN material and its surfaces.

Future work might concern itself with the following activities:

(1) Routine inspection by x-ray diffraction, low energy electron diffraction and more conventional optical studies of all NbN layers used to fabricate NbN tunnel junctions. Correlation of these observations with observed tunnel junction properties should be made.

(2) Careful study of the capacitance of devices measured by Josephson junction techniques and comparison with more conventional

techniques should be made. Further simple extensions of these experiments could accurately measure the London penetration depth in NbN.

(3) A comparison should be made between -

(a) SiO_x barriers

(b) a-Si barriers

(c) CVD Ge barriers

after excellent reproducibility is established on the properties of NbN layers themselves.

(4) More work is needed on the oxidation of NbN. This could lead to more reproducible processing in an oxidization isolation of devices.

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